

FIG.2





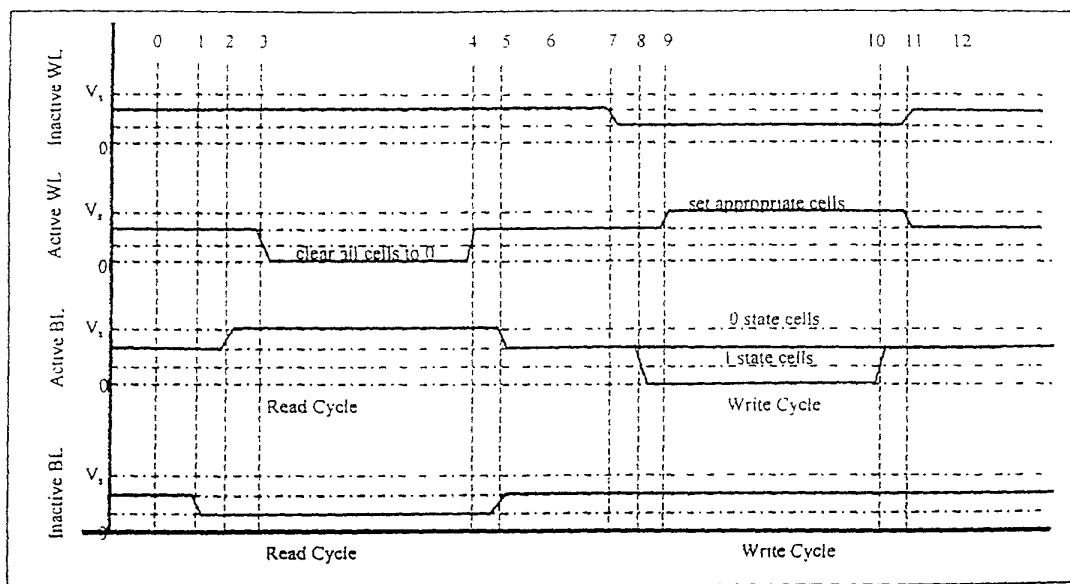


FIG. 6.

10 11 12

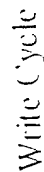


Fig. 7

Five Level Timing Diagram

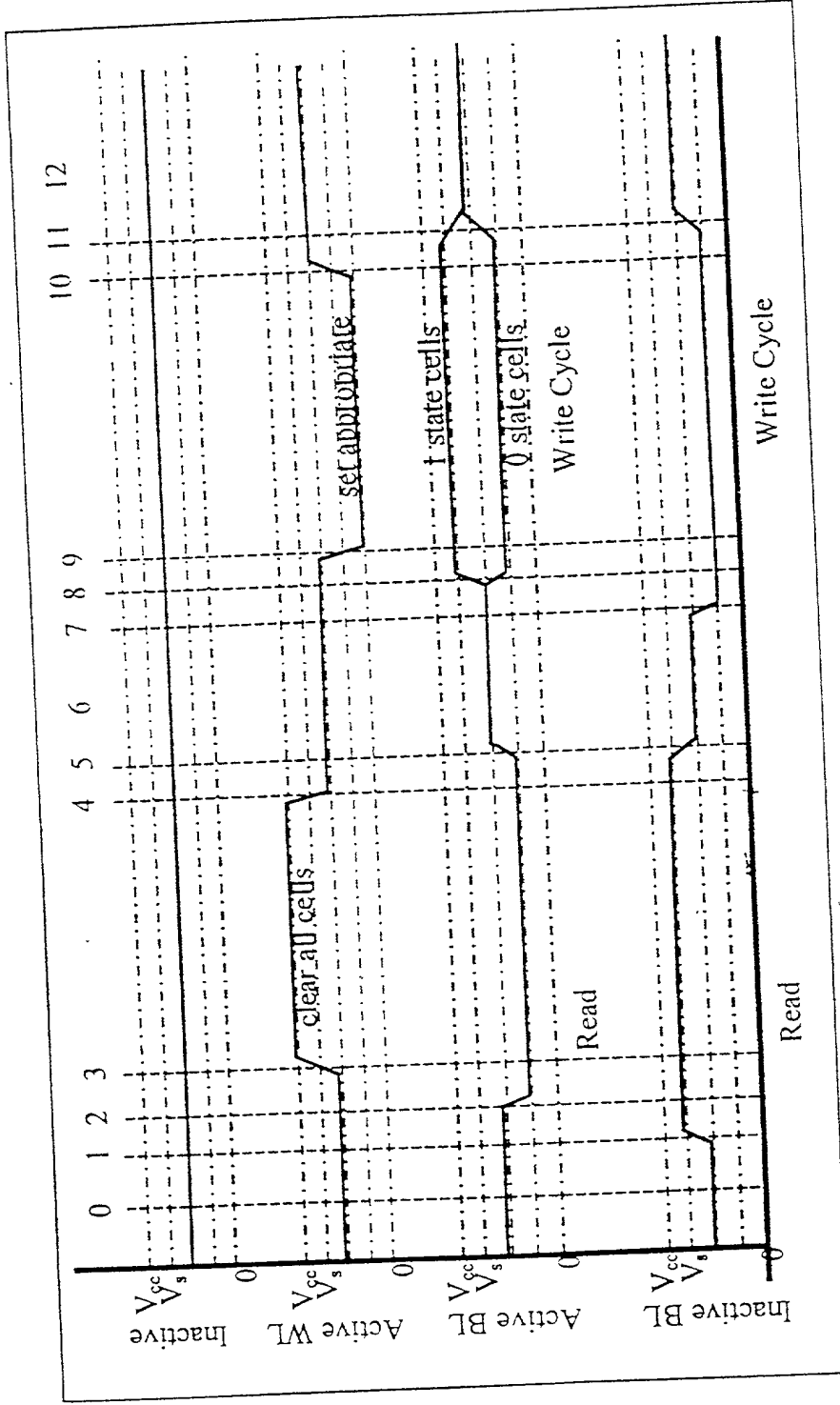


FIG. 9

102201 60000000

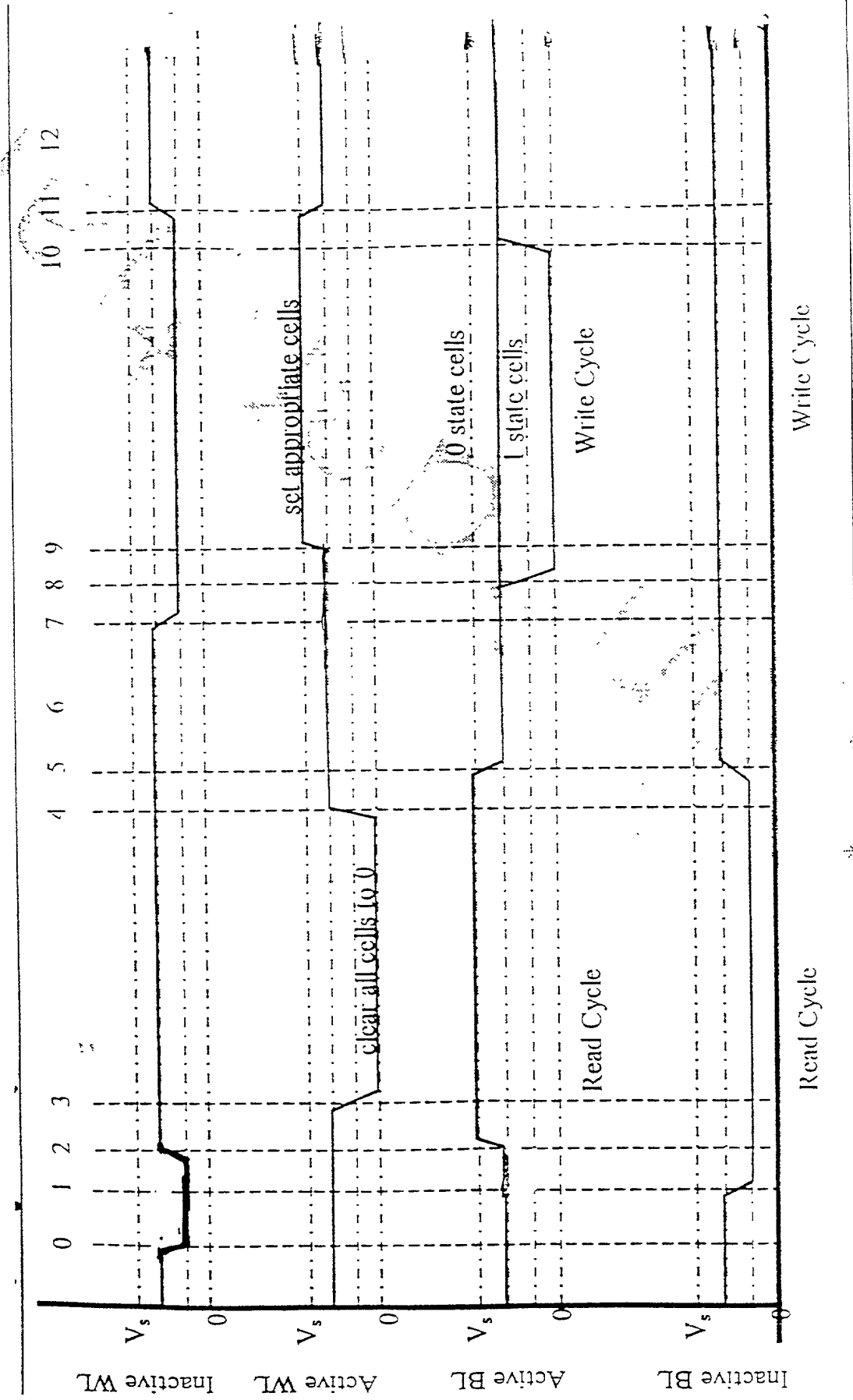


Fig. 10

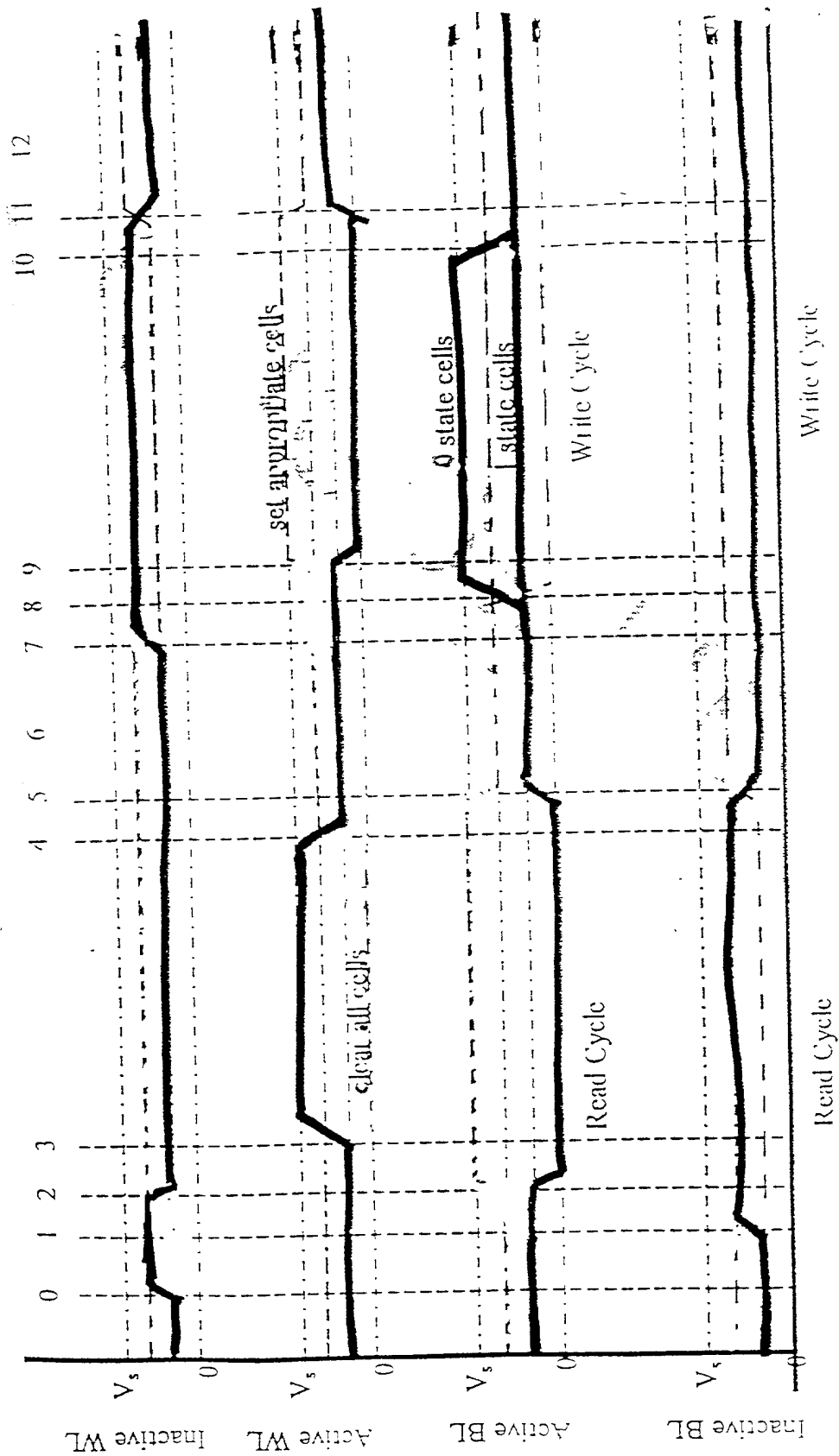


Fig. 11

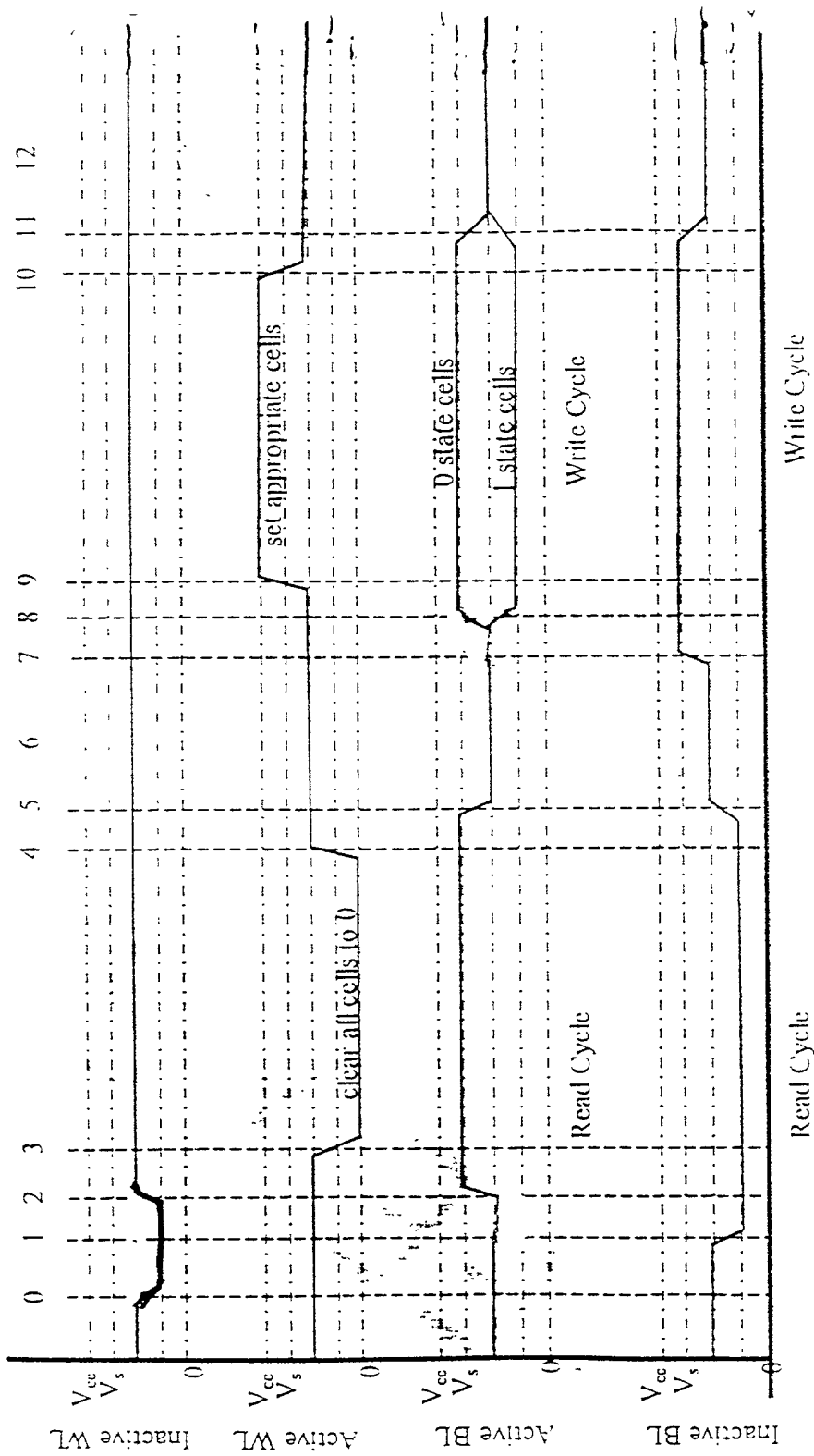


FIG.12

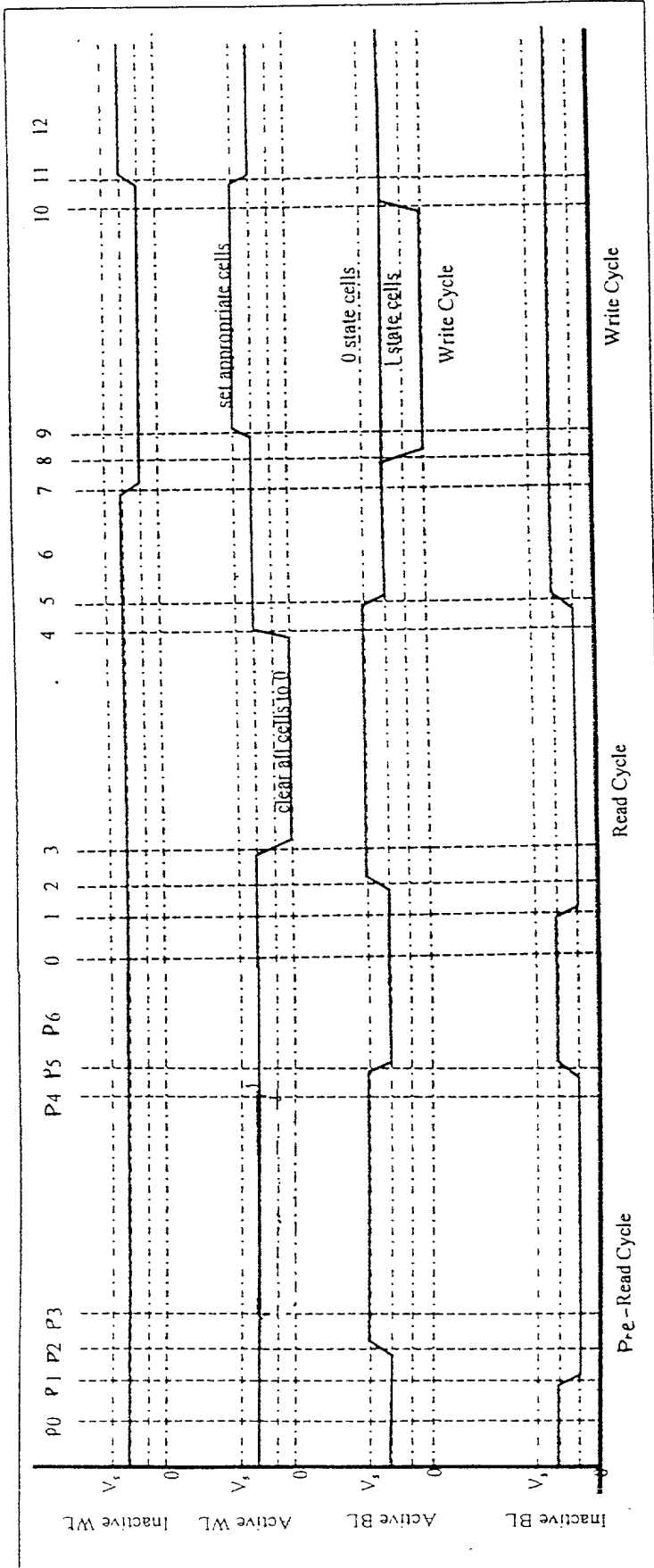


FIG. 14  
EXAMPLE OF READ AND WRITE PROTOCOL INVOLVING A PRE-READ REFERENCE CYCLE.

The diagram illustrates a 1T1C array architecture. It consists of a grid of memory cells. The columns are labeled WL1, WL2, WL3, ..., ACTIVE WL, ..., and SENSE AMPLIFIERS. Each column contains a series of cells. The ACTIVE WL column is highlighted with a thick horizontal bar. The SENSE AMPLIFIERS are represented by triangles at the end of each row.

FIG. 15

BL 1 BL 2 BL 3